GTL2018

8-bit LVTTL to GTL transceiver

Rev. 01 — 15 February 2007 Product data sheet

1. General description

The GTL2018 is an octal translating transceiver designed for 3.3 V LVTTL system interface with a GTL–/GTL/GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-LVTTL sampling receiver or as an LVTTL-to-GTL interface.

The GTL2018 LVTTL inputs (only) are tolerant up to 5.5 V, allowing direct access to TTL or 5 V CMOS inputs.

2. Features

- Operates as an octal GTL–/GTL/GTL+ sampling receiver or as an LVTTL to GTL–/GTL/GTL+ driver
- 3.0 V to 3.6 V operation with 5 V tolerant LVTTL input
- GTL input and output 3.6 V tolerant
- V_{ref} adjustable from 0.5 V to $0.5V_{CC}$
- Partial power-down permitted
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-CC101
- Package offered: TSSOP24

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	control inputs; V_I = 3.0 V or 0 V	-	2	2.5	pF
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V	-	4.6	6	pF
		B port; $V_O = V_{TT}$ or 0 V	-	3.4	4.3	pF
GTL; V_{ref} = 0.8 V; V_{TT} = 1.2 V						
t_{PLH}	LOW-to-HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH-to-LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t_{PLH}	LOW-to-HIGH propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
t_{PHL}	HIGH-to-LOW propagation delay	Bn to An; see Figure 4	-	4.9	7	ns

founded by Philips

4. Ordering information

Table 2. Ordering information

T_{amb} = −40 °C to +85 °C.

Type number	Topside mark	Package		
		Name	Description	Version
GTL2018PW	GTL2018PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

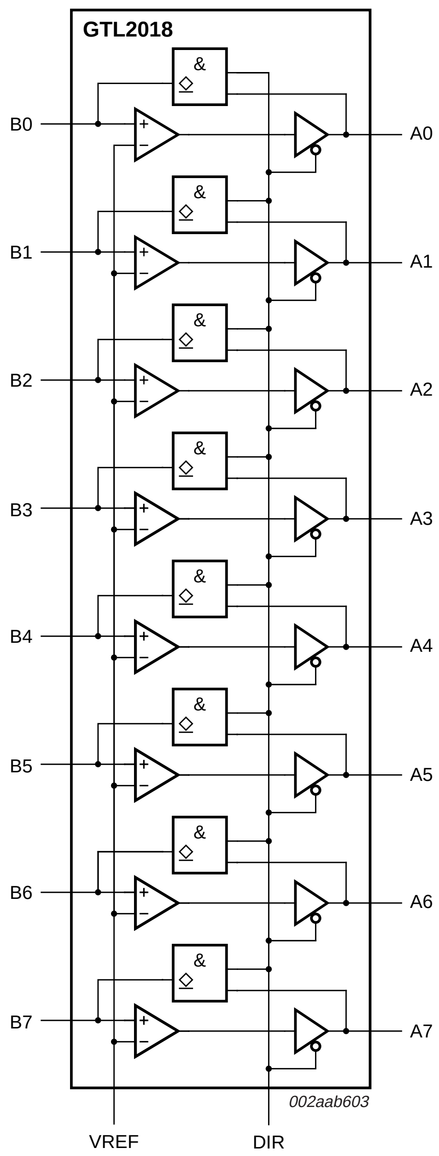


Fig 1. Logic diagram of GTL2018

6. Pinning information

6.1 Pinning

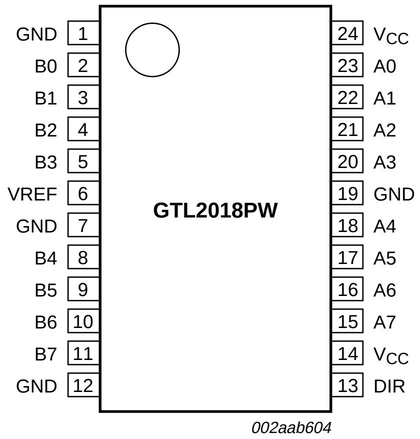


Fig 2. Pin configuration for TSSOP24

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1, 7, 12, 19	ground (0 V)
B0	2	data inputs/outputs (B side, GTL)
B1	3	
B2	4	
B3	5	
B4	8	
B5	9	
B6	10	
B7	11	
VREF	6	GTL reference voltage
DIR	13	direction control input (LVTTL)
V_{CC}	14, 24	positive supply voltage
A7	15	data inputs/outputs (A side, LVTTL)
A6	16	
A5	17	
A4	18	
A3	20	
A2	21	
A1	22	
A0	23	

7. Functional description

Refer to Figure 1 “Logic diagram of GTL2018”.

7.1 Function table

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Input/output	
DIR	An (LVTTL)	Bn (GTL)
H	input	Bn = An
L	An = Bn	input

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage	A port		–0.5[1]	7.0	V
		B port		–0.5[1]	4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	output in OFF or HIGH state; A port		–0.5[1]	7.0	V
		output in OFF or HIGH state; B port		–0.5[1]	4.6	V
I_{OL}	LOW-level output current	A port	[2]	-	32	mA
		B port	[2]	-	80	mA
I_{OH}	HIGH-level output current	A port	[3]	-	–32	mA
T_{stg}	storage temperature		[4]	–60	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] Current into any output in the LOW state.

[3] Current into any output in the HIGH state.

[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.0	-	3.6	V
V_{TT}	termination voltage[2]	GTL–		0.85	0.9	0.95	V
		GTL		1.14	1.2	1.26	V
		GTL+		1.35	1.5	1.65	V
V_{ref}	reference voltage	overall		0.5	$\frac{2}{3}V_{TT}$	$0.5V_{CC}$	V
		GTL–		0.5	0.6	0.63	V
		GTL		0.76	0.8	0.84	V
		GTL+		0.87	1.0	1.10	V
V_I	input voltage	B port		0	V_{TT}	3.6	V
		except B port	[3]	0	3.3	5.5	V
V_{IH}	HIGH-level input voltage	B port		V_{ref} + 0.050	-	-	V
		except B port		2	-	-	V
V_{IL}	LOW-level input voltage	B port		-	-	V_{ref} – 0.050	V
		except B port		-	-	0.8	V
I_{OH}	HIGH-level output current	A port		-	-	–16	mA
I_{OL}	LOW-level output current	B port		-	-	40	mA
		A port		-	-	16	mA
T_{amb}	ambient temperature	operating in free air		–40	-	85	°C

[1] Unused inputs must be held HIGH or LOW to prevent them from floating.

[2] V_{TT} maximum of 3.6 V with resistor sized to so I_{OL} maximum is not exceeded.

[3] A0 to A7 $V_{I(max)}$ is 3.6 V if configured as outputs (DIR = LOW).

10. Static characteristics

Table 7. Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	A port; V_{CC} = 3.0 V to 3.6 V; I_{OH} = –100 μA	[2]	V_{CC} – 0.2	-	-	V
		A port; V_{CC} = 3.0 V; I_{OH} = –16 mA	[2]	2.0	-	-	V
V_{OL}	LOW-level output voltage	B port; V_{CC} = 3.0 V; I_{OL} = 40 mA	[2]	-	0.23	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 8 mA	[2]	-	0.28	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 12 mA	[2]	-	0.40	0.55	V
		A port; V_{CC} = 3.0 V; I_{OL} = 16 mA	[2]	-	0.55	0.8	V
I_I	input current	control inputs; V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	-	±1	μA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND		-	-	±1	μA
		A port; V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	-	10	μA
		A port; V_{CC} = 3.6 V; V_I = V_{CC}		-	-	±1	μA
		A port; V_{CC} = 3.6 V; V_I = 0 V		-	-	–5	μA
I_{OZ}	off-state output current	A port; V_{CC} = 0 V; V_I or V_O = 0 V to 3.6 V		-	-	±100	μA
I_{CC}	supply current	A port; V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 mA		-	8	12	mA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND; I_O = 0 mA		-	8	12	mA
ΔI_{CC}[3]	additional supply current	per input; A port or control inputs; V_{CC} = 3.6 V; V_I = V_{CC} – 0.6 V		-	-	500	μA
C_i	input capacitance	control inputs; V_I = 3.0 V or 0 V		-	2	2.5	pF
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V		-	4.6	6	pF
		B port; V_O = V_{TT} or 0 V		-	3.4	4.3	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The input and output voltage ratings my be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

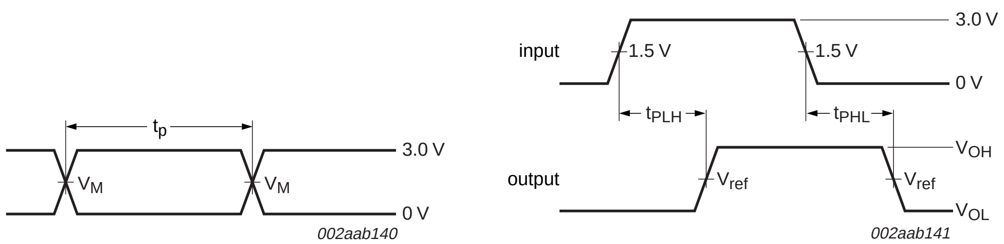
V_{CC} = 3.3 V ± 0.3 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
GTL−; V_{ref} = 0.6 V; V_{TT} = 0.9 V						
t_{PLH}	LOW-to-HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH-to-LOW propagation delay	An to Bn; see Figure 3	-	3.3	7	ns
t_{PLH}	LOW-to-HIGH propagation delay	Bn to An; see Figure 4	-	5.3	8	ns
t_{PHL}	HIGH-to-LOW propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
GTL; V_{ref} = 0.8 V; V_{TT} = 1.2 V						
t_{PLH}	LOW-to-HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH-to-LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t_{PLH}	LOW-to-HIGH propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
t_{PHL}	HIGH-to-LOW propagation delay	Bn to An; see Figure 4	-	4.9	7	ns
GTL+; V_{ref} = 1.0 V; V_{TT} = 1.5 V						
t_{PLH}	LOW-to-HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH-to-LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t_{PLH}	LOW-to-HIGH propagation delay	Bn to An; see Figure 4	-	5.1	8	ns
t_{PHL}	HIGH-to-LOW propagation delay	Bn to An; see Figure 4	-	4.7	7	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11.1 Waveforms

V_M = 1.5 V at $V_{CC} \geq 3.0$ V; $V_M = 0.5V_{CC}$ at $V_{CC} \leq 2.7$ V for A ports and control pins; $V_M = V_{ref}$ for B ports.



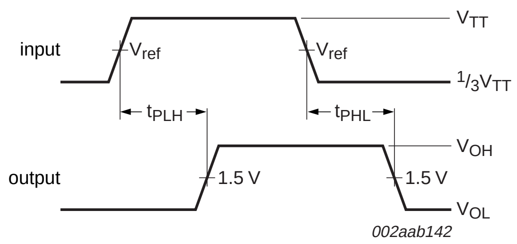
V_M = 1.5 V for A port and V_{ref} for B port

a. Pulse duration

A port to B port

b. Propagation delay times

Fig 3. Voltage waveforms



PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns

Fig 4. Propagation delay, Bn to An

12. Test information

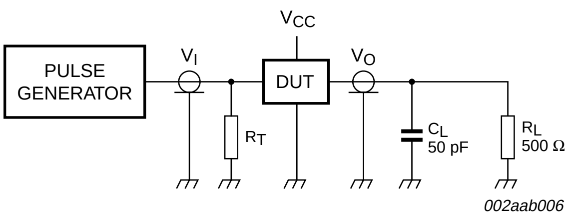
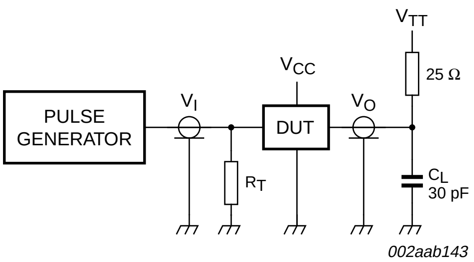


Fig 5. Load circuitry for switching times



R_L = load resistor.

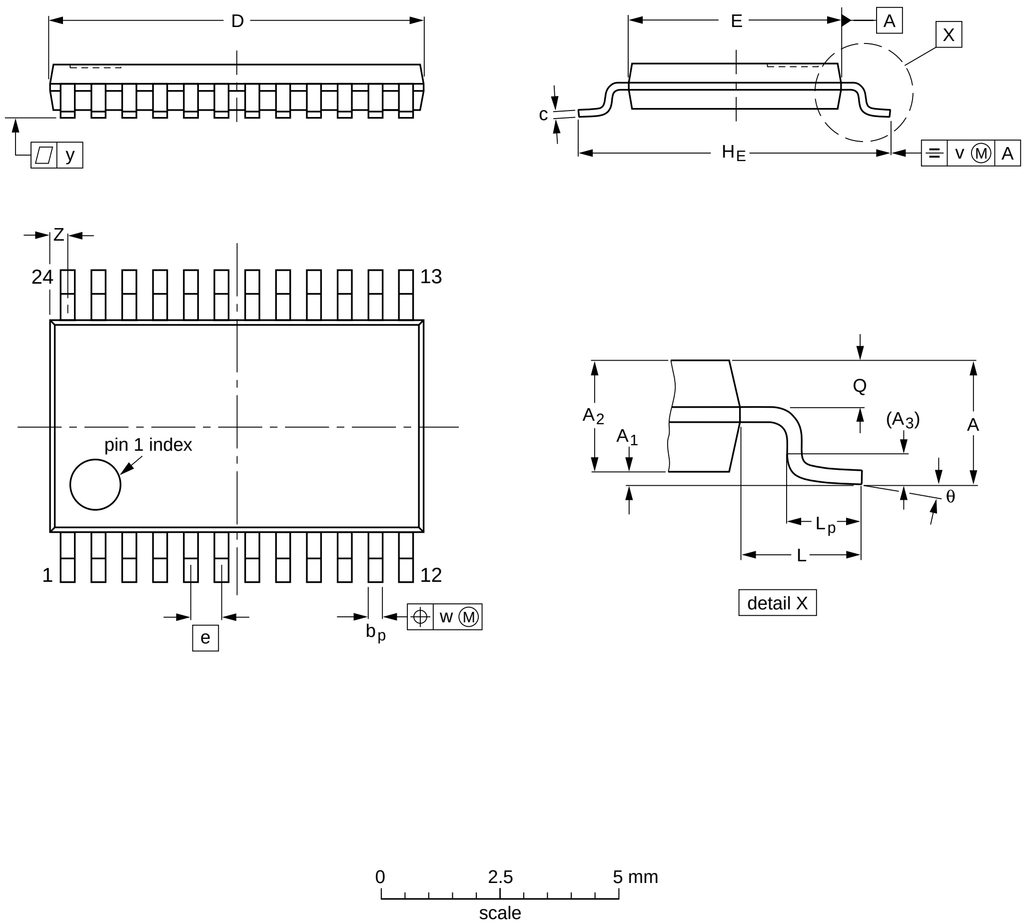
C_L = load capacitance; includes jib and probe capacitance.

R_T = termination resistance; should be equal to Z_o of pulse generators.

Fig 6. Load circuit for B outputs

13. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT355-1 (TSSOP24)

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

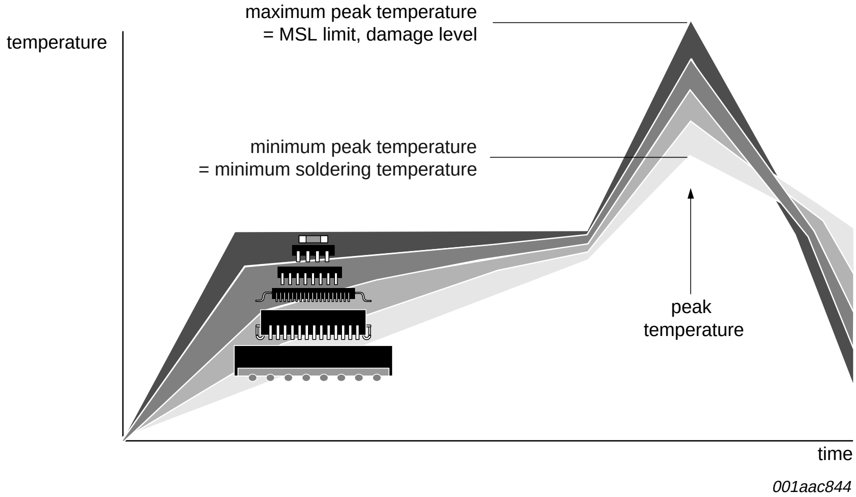
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Repetition Rate
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2018_1	20070215	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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19. Contents

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